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US 6713838 B2	20040330	Inductive fuse for semiconductor device	257/529	257/E23.149	Pricer; Wilbur et al.
US 6693597 B2	20040217	Layout for automotive window antenna	343/713	343/704	Walton; Eric K al.
US 6689650 B2	20040210	Fin field effect transistor with self-aligned gate	438/157	257/302; 257/E21.415; 257/E21.442; 257/E29.137; 257/E29.275; 257/E29.283; 257/E29.299; 438/159; 438/163; 438/206; 438/242;	Gambino; Jeff P. et al.

				438/279; 438/283	
US 6674168 B1	20040106	Single and multilevel rework	257/758	257/752; 257/759; 257/760; 257/762; 257/E21.576; 257/E21.579; 257/E21.595; 257/E23.146; 257/E23.167; 438/4	Cooney, III; Edward C. et al.
US 6674134 B2	20040106	Structure and method for dual gate oxidation for CMOS technology	257/397	257/396; 257/510; 257/E21.546; 257/E21.625; 257/E21.628; 438/427	Berry; Wayne al.
US 6670255 B2	20031230	Method of fabricating lateral diodes and bipolar transistors	438/343	257/586; 257/587; 257/E27.022; 257/E27.112	Adkisson; Jam W. et al.
US 6667533 B2	20031223	Triple damascene fuse	257/529	257/296; 257/642; 257/643; 257/E23.149; 257/E23.167; 438/132; 438/215; 438/281; 438/333	Daubenspeck; Timothy H. et
US 6661106 B1	20031209	Alignment mark structure for laser fusing and method of use	257/797	257/665; 257/750; 257/774; 257/E23.15; 257/E23.179	Gilmour; Rich A. et al.
US 6614922 B1	20030902	Wire pattern test system	382/141	348/86	Walton; Eric K
US 6605534 B1	20030812	Selective deposition of a conductive material	438/674	257/E21.175; 257/E21.586; 438/638; 438/677; 438/678; 438/687; 438/799	Chung; Dean S al.
US 6605526	20030812	Wirebond passivation pad	438/618	252/390;	Howell; Wayn

B1		connection using heated capillary		257/E21.508; 257/E21.519; 257/E21.582; 257/E23.02; 438/695; 438/734	John et al.
US 6595920 B2	20030722	Non-contact instrument for measurement of internal optical pressure	600/401	600/402	Walton; Eric K
US 6590259 B2	20030708	Semiconductor device of an embedded DRAM on SOI substrate	257/347	257/354; 257/67; 257/69; 257/E21.652; 257/E21.703; 257/E27.112	Adkisson; Jam W. et al.
US 6573538 B2	20030603	Semiconductor device with internal heat dissipation	257/127	257/707; 257/720; 257/722; 257/E23.105	Motsiff; Willia T. et al.
US 6559543 B1	20030506	Stacked fill structures for support of dielectric layers	257/758	257/E23.167; 257/E23.194; 438/622	Dunham; Timc G. et al.
US 6548357 B2	20030415	Modified gate processing for optimized definition of array and logic devices on same chip	438/279	257/E21.507; 257/E21.624; 257/E21.645; 257/E21.66; 438/200; 438/241; 438/275	Weybright; Ma E. et al.
US 6538295 B1	20030325	Salicide device with borderless contact	257/412	257/384; 257/388; 257/413; 257/E21.438	Bronner; Gary et al.
US 6518670 B1	20030211	Electrically porous on-chip decoupling/shielding layer	257/752	257/750; 257/758; 257/763; 257/764; 257/774; 257/E21.507; 257/E23.144; 257/E23.153; 257/E27.047; 257/E27.048	Mandelman; Je A. et al.
US 6518119 B2	20030211	Strap with intrinsically conductive barrier	438/243	257/E21.653; 257/E29.346; 438/386	Gambino; Jeffi P. et al.

US 6512292 B1	20030128	Semiconductor chip structures with embedded thermal conductors and a thermal sink disposed over opposing substrate surfaces	257/712	257/347; 257/E23.105; 257/E23.144; 257/E23.167	Armbrust; Douglas S. et al.
US 6504210 B1	20030107	Fully encapsulated damascene gates for Gigabit DRAMs	257/344	257/408; 257/E21.198; 257/E21.434; 257/E29.157; 438/230; 438/284; 438/592; 438/596	Divakaruni; Ramachandra C.
US 6504203 B2	20030107	Method of forming a metal-insulator-metal capacitor for dual damascene interconnect processing and the device so formed	257/303	257/E21.009	Gambino; Jeffrey P. et al.
US 6503798 B1	20030107	Low resistance strap for high density trench DRAMS	438/268	257/301; 257/305; 257/E21.653; 438/234; 438/243; 438/253	Divakaruni; Ramachandra C.
US 6501131 B1	20021231	Transistors having independently adjustable parameters	257/344	257/345; 257/773; 257/E21.434; 257/E21.437; 257/E21.443; 257/E21.507; 257/E21.59; 257/E21.633; 438/289; 438/291	Divakaruni; Ramachandra C. et al.
US 6498385 B1	20021224	Post-fuse blow corrosion prevention structure for copper fuses	257/529	257/536; 257/537; 257/758; 257/762; 257/E21.579; 257/E21.584; 257/E21.585; 257/E23.15	Daubenspeck; Timothy H. et al.
US 6498056 B1	20021224	Apparatus and method for antifuse with electrostatic	438/131	257/50; 257/529;	Motsiff; William T. et al.

		assist		257/530; 257/E23.147; 257/E23.148; 438/467; 438/600	
US 6496053 B1	20021217	Corrosion insensitive fusible link using capacitance sensing for semiconductor devices	327/525	257/173; 257/516; 257/529; 257/530; 257/532; 257/665; 257/910; 257/E21.008; 257/E23.15; 361/628; 361/630; 438/132; 438/215; 438/467	Daubenspeck; Timothy et al.
US 6495439 B1	20021217	Method for suppressing pattern distortion associated with BPSG reflow and integrated circuit chip formed thereby	438/597	257/E21.279; 257/E21.576; 257/E23.167; 438/602; 438/760; 438/763	Gambino; Jeff Peter et al.
US 6492207 B2	20021210	Method for making a pedestal fuse	438/132	257/E23.15	Bouldin; Denn et al.
US 6486505 B1	20021126	Semiconductor contact and method of forming the same	257/306	257/309; 257/768; 257/E21.654	Rupp; Thomas et al.
US 6483468 B2	20021119	On-glass impedance matching antenna connector	343/713		Walton; Eric K
US 6479368 B1	20021112	Method of manufacturing a semiconductor device having a shallow trench isolating region	438/435	257/E21.546; 438/424; 438/443; 438/444; 438/445	Mandelman; J. A. et al.
US 6472230 B2	20021029	Re-settable tristate programmable device	438/3	257/E23.15; 438/131; 438/132	Kimmel; Kurt et al.
US 6471845 B1	20021029	Method of controlling chemical bath composition in a manufacturing environment	205/81	137/93; 205/101	Dukovic; John et al.
US 6458630	20021001	Antifuse for use with low	438/131	257/E23.148;	Daubenspeck;

B1		k dielectric foam insulators		257/E23.167; 438/600; 438/610; 438/781	Timothy H. et
US 6455914 B2	20020924	Pedestal fuse	257/529	257/536; 257/537; 257/752; 257/762; 257/E23.15	Bouldin; Denn et al.
US 6448173 B1	20020910	Aluminum-based metallization exhibiting reduced electromigration and method therefor	438/627	257/E21.582; 257/E21.584; 257/E21.585; 257/E23.16; 438/688	Clevenger; Lawrence Alfr et al.
US 6440834 B2	20020827	Method and structure for a semiconductor fuse	438/601	257/529; 257/E23.15; 438/132; 438/600	Daubenspeck; Timothy Harri: et al.
US 6437748 B1	20020820	Tapered anechoic chamber	343/703	324/627; 342/1	Burnside; Wal D. et al.
US 6436749 B1	20020820	Method for forming mixed high voltage (HV/LV) transistors for CMOS devices using controlled gate depletion	438/199	257/E21.637; 257/E27.062; 438/261; 438/263	Tonti; William et al.
US 6429474 B1	20020806	Storage-capacitor electrode and interconnect	257/296	257/306; 257/758; 257/E21.657; 257/E21.66; 257/E23.142 CIPG 20060101 A H01L H01L21/02 L N R US M 20060101 CICL H01L CIPN H01L21/02 20060101 CIPG 20060101 A H01L H01L21/02 L N R US M 20060101	Gambino; Jeff P. et al.

				CICL H01L CIPN H01L21/02 20060101 CIPG 20060101 A H01L H01L21/70 L I R US M 20060101 CICL H01L CIPS; H01L21/70 20060101 CIPG 20060101 A H01L H01L21/8242 L I R US M 20060101 CICL H01L CIPS H01L21/8242 20060101	
US 6426557 B1	20020730	Self-aligned last-metal C4 interconnection layer for Cu technologies	257/750	257/760; 257/761; 257/774; 257/E23.02	Daubenspeck; Timothy et al.
US 6426247 B1	20020730	Low bitline capacitance structure and method of making same	438/185	257/E21.658; 438/740; 438/761	Divakaruni; Ramachandra c
US 6420772 B1	20020716	Re-settable tristate programmable device	257/529	257/E23.15	Kimmel; Kurt et al.
US 6420749 B1	20020716	Trench field shield in trench isolation	257/301	257/308; 257/510; 257/E21.538; 257/E21.549; 257/E21.59; 257/E21.627; 257/E21.628; 438/424; 438/440	Divakaruni; Ramachandra c
US 6413870 B1	20020702	Process of removing CMP scratches by BPSG reflow and integrated circuit chip formed thereby	438/692	216/89; 257/E21.243; 257/E21.244; 257/E21.271;	Gambino; Jeff P. et al.

				257/E21.576; 438/694; 438/698; 438/760	
US 6409903 B1	20020625	Multi-step potentiostatic/galvanostatic plating control	205/96	204/229.5; 204/DIG.9; 205/105; 205/157; 205/291	Chung; Dean S al.
US 6403423 B1	20020611	Modified gate processing for optimized definition of array and logic devices on same chip	438/279	257/E21.507; 257/E21.624; 257/E21.645; 257/E21.66; 438/200; 438/241; 438/275	Weybright; Ma E. et al.
US 6396151 B1	20020528	Partially-overlapped interconnect structure and method of making	257/762	257/765; 257/771; 257/E23.145; 257/E23.159	Colgan; Evan George et al.
US 6395594 B2	20020528	Method for simultaneously forming a storage- capacitor electrode and interconnect	438/238	257/E21.656; 257/E21.66; 438/622	Kotecki; David et al.
US 6380027 B2	20020430	Dual tox trench dram structures and process using V-groove	438/241	257/E21.655; 257/E27.091; 257/E27.092; 438/271; 438/296; 438/386	Furukawa; Toshiharu et al
US 6375159 B2	20020423	High laser absorption copper fuse and method for making the same	257/529	257/762; 257/764; 257/E23.15	Daubenspeck; Timothy H. et
US 6369423 B2	20020409	Semiconductor device with a thin gate stack having a plurality of insulating layers	257/327	257/332; 257/338; 257/369; 257/635; 257/750; 257/E21.507	Ohiwa; Tokuh et al.
US 6350653 B1	20020226	Embedded DRAM on silicon-on-insulator substrate	438/258	257/E21.652; 257/E21.703; 257/E27.112; 438/149; 438/266; 438/275; 438/279	Adkisson; Jam W. et al.

US 6344389 B1	20020205	Self-aligned damascene interconnect	438/244	257/E21.579; 257/E21.649; 257/E21.657; 438/239; 438/396; 438/397; 438/595 CIPG 20060101 A H01L H01L21/70 L I R US M 20060101 CICL H01L CIPS H01L21/70 20060101 CIPG 20060101 A H01L H01L21/8242 L I R US M 20060101 CICL H01L CIPS H01L21/8242 20060101 CIPG 20060101 A H01L H01L27/108 L N R US M 20060101 CICL H01L CIPN; H01L27/108 20060101 CIPG 20060101 A H01L H01L27/108 L N R US M 20060101 CICL H01L CIPN H01L27/108	Bronner; Gary et al.
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US 6344383 B1	20020205	Structure and method for dual gate oxidation for CMOS technology	438/221	257/E21.546; 257/E21.625; 257/E21.628; 438/218; 438/275; 438/279; 438/424	Berry; Wayne al.
US 6340630 B1	20020122	Method for making interconnect for low temperature chip attachment	438/613	257/E21.511; 438/612; 438/614; 438/616	Berger; Daniel George et al.
US 6339001 B1	20020115	Formulation of multiple gate oxides thicknesses without exposing gate oxide or silicon surface to photoresist	438/275	257/E21.625; 438/287; 438/981	Bronner; Gary et al.
US 6335229 B1	20020101	Inductive fuse for semiconductor device	438/132	257/529; 257/E23.149	Pricer; Wilbur et al.
US 6326260 B1	20011204	Gate pre-spacers for high density, high performance DRAMs	438/241	257/E21.625; 257/E21.66; 438/592; 438/595; 438/700	Divakaruni; Ramachandra et al.
US 6320558 B1	20011120	On-glass impedance matching antenna connector	343/906	343/860; 343/904	Walton; Eric K
US 6274467 B1	20010814	Dual work function gate conductors with self-aligned insulating cap	438/563	257/E21.197; 257/E21.199; 257/E21.316; 257/E21.637; 438/301	Gambino; Jeff P. et al.
US 6270646 B1	20010807	Electroplating apparatus and method using a compressible contact	205/93	204/224R; 205/117; 205/118; 205/123; 205/157; 205/98	Walton; Erick Gregory et al.
US 6261950 B1	20010717	Self-aligned metal caps for interlevel metal connections	438/641	257/E21.591; 257/E23.145; 438/626; 438/633; 438/660; 438/661; 438/674; 438/681;	Tobben; Dirk et al.

				438/685; 438/688	
US 6261914 B1	20010717	Process for improving local uniformity of chemical mechanical polishing using a self-aligned polish rate enhancement layer	438/359	257/E21.244; 257/E21.548; 438/360	Divakaruni; Ramachandra
US 6261873 B1	20010717	Pedestal fuse	438/132	257/E23.15; 438/215; 438/281; 438/333	Bouldin; Denn et al.
US 6259129 B1	20010710	Strap with intrinsically conductive barrier	257/304	257/301; 257/302; 257/303; 257/305; 257/306; 257/E21.653; 257/E29.346	Gambino; Jeff P. et al.
US 6258689 B1	20010710	Low resistance fill for deep trench capacitor	438/386	257/301; 257/304; 257/516; 257/61; 257/E21.396; 257/E21.651; 438/243; 438/246; 438/362	Bronner; Gary et al.
US 6252271 B1	20010626	Flash memory structure using sidewall floating gate and method for forming the same	257/315	257/316; 257/317; 257/E21.209; 257/E21.422; 257/E27.103; 257/E29.129; 257/E29.304	Gambino; Jeff P. et al.
US 6249038 B1	20010619	Method and structure for a semiconductor fuse	257/529	257/209; 257/E23.15	Daubenspeck; Timothy Harri et al.
US 6236077 B1	20010522	Trench electrode with intermediate conductive barrier layer	257/301	257/305; 257/E21.396; 257/E21.653; 257/E29.346	Gambino; Jeff P. et al.
US 6232222 B1	20010515	Method of eliminating a critical mask using a blockout mask and a resulting semiconductor	438/637	257/E21.257; 257/E21.507; 438/258; 438/671	Armacost; Mic et al.

		structure			
US 6222219 B1	20010424	Crown capacitor using a tapered etch of a damascene lower electrode	257/306	257/303; 257/E21.648	Gambino; Jeff P. et al.
US 6210995 B1	20010403	Method for manufacturing fusible links in a semiconductor device	438/132	257/E23.149	Brintzinger; A. C. et al.
US 6208008 B1	20010327	Integrated circuits having reduced stress in metallization	257/510	257/513; 257/E21.576; 257/E21.578; 257/E21.589	Arndt; Kennetl et al.
US 6204532 B1	20010320	Pillar transistor incorporating a body contact	257/329	257/330; 257/332; 257/347; 257/E21.41; 257/E29.262; 257/E29.274	Gambino; Jeff Peter et al.
US 6201272 B1	20010313	Method for simultaneously forming a storage-capacitor electrode and interconnect	257/296	257/750; 257/E21.656; 257/E21.66	Kotecki; David et al.
US 6200834 B1	20010313	Process for fabricating two different gate dielectric thicknesses using a polysilicon mask and chemical mechanical polishing (CMP) planarization	438/142	257/E21.622; 257/E21.623; 257/E21.625; 438/303; 438/305	Bronner; Gary et al. □
US 6194755 B1	20010227	Low-resistance salicide fill for trench capacitors	257/301	257/E21.651; 438/243; 438/386	Gambino; Jeff P. et al.
US 6177348 B1	20010123	Low temperature via fill using liquid phase transport	438/677	257/E21.588; 438/660; 438/926	Gambino; Jeff P. et al.
US 6174762 B1	20010116	Salicide device with borderless contact	438/230	257/413; 257/E21.438; 438/592; 438/595	Bronner; Gary et al.
US 6174756 B1	20010116	Spacers to block deep junction implants and silicide formation in integrated circuits	438/163	257/E21.619; 257/E21.646; 438/184; 438/514	Gambino; Jeff P. et al.
US 6166423 A	20001226	Integrated circuit having a via and a capacitor	257/532	257/535; 257/E21.009; 257/E21.011; 257/E21.579;	Gambino; Jeff P. et al.

				257/E21.647; 257/E27.048 CIPG 20060101 A H01L H01L21/02 L I R US M 20060101 CICL H01L CIPS H01L21/02 20060101 CIPG 20060101 A H01L H01L21/02 L I R US M 20060101 CICL H01L CIPS H01L21/02 20060101 CIPG 20060101 A H01L H01L21/70 L I R US M 20060101 CICL H01L CIPS; H01L21/70 20060101 CIPG 20060101 A H01L H01L21/768 L N R US M 20060101 CICL H01L CIPN H01L21/768 20060101 CIPG 20060101 A H01L H01L21/8242	
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US 6165896 A	20001226	Self-aligned formation and method for semiconductors	438/636	257/E21.577; 438/514; 438/526; 438/586; 438/593; 438/595	Schnabel; Rair F. et al.
US 6150212 A	20001121	Shallow trench isolation method utilizing combination of spacer and fill	438/244	257/E21.549; 438/400; 438/427	Divakaruni; Ramachandra
US 6136686 A	20001024	Fabrication of interconnects with two different thicknesses	438/624	257/E21.507; 257/E21.579; 438/638; 438/668; 438/783	Gambino; Jeff P. et al.
US 6136655 A	20001024	Method of making low voltage active body semiconductor device	438/289	257/E21.415; 257/E21.654; 257/E21.703; 257/E29.281; 438/592;	Assaderaghi; Fariborz et al.

				438/596	
US 6127735 A	20001003	Interconnect for low temperature chip attachment	257/778	257/737; 257/779; 257/E21.511	Berger; Daniel George et al.
US 6124199 A	20000926	Method for simultaneously forming a storage-capacitor electrode and interconnect	438/622 CIPG 20060101 A H01L H01L21/02 L N R US M 20060101 CICL H01L CIPN H01L21/02 20060101 CIPG 20060101 A H01L H01L21/02 L N R US M 20060101 CICL H01L CIPN H01L21/02 20060101 CIPG 20060101 A H01L H01L21/70 L I R US M 20060101 CICL H01L CIPS H01L21/70 20060101 CIPG 20060101 A H01L H01L21/8242 L I R US M 20060101 CICL H01L CIPS H01L21/8242 20060101	257/239; 257/396; 257/E21.657; 257/E21.66; 257/E23.142; 438/239; 438/241; 438/253; 438/396; 438/399	Gambino; Jeff P. et al.
US 6114248	20000905	Process to reduce localized	438/692	257/E21.304;	Gambino; Jeff

A		polish stop erosion		438/693	P. et al.
US 6110832 A	20000829	Method and apparatus for slurry polishing	438/692	156/345.12; 216/88; 216/89; 438/693; 438/745	Morgan, III; Clifford O. et al.
US 6097345 A	20000801	Dual band antenna for vehicles	343/769	343/700MS; 343/711; 343/713	Walton; Eric K
US 6096664 A	20000801	Method of manufacturing semiconductor structures including a pair of MOSFETs	438/275	257/390; 257/E21.625; 438/279; 438/296	Rupp; Thomas et al.
US 6093630 A	20000725	Semi-conductor personalization structure and method	438/612	228/180.21; 228/180.22; 257/E23.021; 257/E23.146; 438/613	Geffken; Robe Michael et al.
US 6090671 A	20000718	Reduction of gate-induced drain leakage in semiconductor devices	438/291	257/E21.194; 257/E21.324; 257/E21.433; 438/530; 438/910	Balasubramany Karanam et al.
US 6084276 A	20000704	Threshold voltage tailoring of corner of MOSFET device	257/397	257/394; 257/404; 257/513; 257/519; 257/E21.548; 257/E21.551; 257/E21.618; 438/296; 438/424; 438/430; 438/433	Gambino; Jeff Peter et al.
US 6081021 A	20000627	Conductor-insulator-conductor structure	257/530	257/209; 257/529; 257/E21.008; 257/E21.011; 257/E21.582	Gambino; Jeff P. et al.
US 6060746 A	20000509	Power transistor having vertical FETs and method for making same	257/331	257/334; 257/401; 257/E21.41; 257/E21.419; 257/E29.131; 257/E29.26; 257/E29.262	Bertin; Claude et al.

US 6054339 A	20000425	Fusible links formed on interconnects which are at least twice as long as they are deep	438/132	257/E23.15; 438/601; 438/618	Gilmour; Rich: A. et al.
US 6037648 A	20000314	Semiconductor structure including a conductive fuse and process for fabrication thereof	257/529	257/E21.589; 257/E23.149	Arndt; Kennetl et al.
US 6028004 A	20000222	Process for controlling the height of a stud intersecting an interconnect	438/657	257/E21.582; 257/E21.589; 438/618; 438/631; 438/633; 438/637; 438/652; 438/666; 438/669; 438/672; 438/700	Bronner; Gary et al.
US 6025226 A	20000215	Method of forming a capacitor and a capacitor formed using the method	438/244	257/E21.009; 257/E21.011; 257/E21.579; 257/E21.647; 257/E27.048; 438/600; 438/633 CIPG 20060101 A H01L H01L21/02 L I R US M 20060101 CICL H01L CIPS H01L21/02 20060101 CIPG 20060101 A H01L H01L21/02 L I R US M 20060101 CICL H01L CIPS H01L21/02 20060101	Gambino; Jeffi P. et al.

				CIPG 20060101 A H01L H01L21/70 L I R US M 20060101 CICL H01L CIPS H01L21/70; 20060101 CIPG 20060101 A H01L H01L21/768 L N R US M 20060101 CICL H01L CIPN H01L21/768 20060101 CIPG 20060101 A H01L H01L21/8242 L I R US M 20060101 CICL H01L CIPS H01L21/8242 20060101 CIPG 20060101 A H01L H01L27/08 L I R US M 20060101 CICL H01L CIPS; H01L27/08 20060101 CIPG 20060101 A H01L H01L27/08 L I R US M 20060101	
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US 6020239 A	20000201	Pillar transistor incorporating a body contact	438/269	257/E21.41; 257/E29.262; 257/E29.274; 438/192; 438/268; 438/416; 438/621	Gambino; Jeffi Peter et al.
US 6015991 A	20000118	Asymmetrical field effect transistor	257/336	257/344; 257/401; 257/408; 257/654; 257/E21.314; 257/E21.346; 257/E21.427; 257/E21.444; 257/E29.135; 257/E29.268	Wheeler; Dona C. et al.
US 6014310 A	20000111	High dielectric TiO.sub.2 - SiN composite films for memory applications	361/311	257/E21.268; 361/321.5; 361/322; 427/79; 427/81	Bronner; Gary Bela et al.
US 6013583 A	20000111	Low temperature BPSG deposition process	438/783	257/E21.243; 257/E21.275; 438/787; 438/790	Ajmera; Atul C al.
US 6004837 A	19991221	Dual-gate SOI transistor	438/157	257/E29.275; 438/159	Gambino; Jeffi P. et al.
US 5998847 A	19991207	Low voltage active body semiconductor device	257/401	257/217; 257/392; 257/403; 257/900; 257/E21.415; 257/E21.654; 257/E21.703; 257/E29.281	Assaderaghi; Fariborz et al.
US 5997392 A	19991207	Slurry injection technique for chemical-mechanical polishing	451/446	451/287	Chamberlin; Timothy S. et al.
US 5994215 A	19991130	Method for suppression pattern distortion associated with BPSG	438/624	257/760; 257/E21.576; 438/760	Gambino; Jeffi Peter et al.

		reflow			
US 5994202 A	19991130	Threshold voltage tailoring of the corner of a MOSFET device	438/433	257/354; 257/374; 257/386; 257/E21.548; 257/E21.551; 257/E21.618; 438/296; 438/424; 438/430	Gambino; Jeffi Peter et al.
US 5973385 A	19991026	Method for suppressing pattern distortion associated with BPSG reflow and integrated circuit chip formed thereby	257/644	257/650; 257/760; 257/E21.279; 257/E21.576; 257/E23.167; 428/210	Gambino; Jeffi Peter et al.
US 5960318 A	19990928	Borderless contact etch process with sidewall spacer and selective isotropic etch process	438/637	257/E21.577; 438/639; 438/695	Peschke; Mattl L. et al.
US 5960315 A	19990928	Tapered via using sidewall spacer reflow	438/632	257/E21.578; 438/648; 438/688; 438/696; 438/908	Gambino; Jeffi P. et al.
US 5939335 A	19990817	Method for reducing stress in the metallization of an integrated circuit	438/696	257/E21.311; 257/E21.576; 257/E21.578; 257/E21.589; 438/700; 438/710; 438/714	Arndt; Kennetl et al.
US 5937289 A	19990810	Providing dual work function doping	438/233	257/E21.197; 257/E21.623; 438/231; 438/525; 438/556; 438/563	Bronner; Gary Bela et al.
US 5923991 A	19990713	Methods to prevent divot formation in shallow trench isolation areas	438/424	257/E21.546; 438/696; 438/697	Bronner; Gary Bela et al.
US 5915183 A	19990622	Raised source/drain using recess etch of polysilicon	438/300	257/E21.206; 257/E21.304; 257/E21.434; 257/E21.59; 257/E29.122;	Gambino; Jeffi P. et al.

				438/649; 438/683	
US 5897336 A	19990427	Direct chip attach for low alpha emission interconnect system	438/108	257/E21.514; 257/E23.115; 438/613	Brouillette; Gu Paul et al.
US 5885899 A	19990323	Method of chemically mechanically polishing an electronic component using a non-selective ammonium hydroxide slurry	438/693	252/79.1; 257/E21.304; 438/697	Armacost; Mic David et al.
US 5883435 A	19990316	Personalization structure for semiconductor devices	257/758	257/734; 257/737; 257/779; 257/780; 257/E23.021; 257/E23.146	Geffken; Robe Michael et al.
US 5882992 A	19990316	Method for fabricating Tungsten local interconnections in high density CMOS circuits	438/582	257/360; 257/E21.59; 438/647; 438/648	Kobeda; Edwa al.
US 5879985 A	19990309	Crown capacitor using a tapered etch of a damascene lower electrode	438/253	257/E21.648; 438/240; 438/396	Gambino; Jeffi P. et al.
US 5877589 A	19990302	Gas discharge devices including matrix materials with ionizable gas filled sealed cavities	313/582	313/234; 313/584; 313/586; 313/607; 445/24; 445/25	Morgan; Cliffe O. et al.
US 5876788 A	19990302	High dielectric TiO.sub.2 - SiN composite films for memory applications	427/81	216/6; 257/E21.268; 427/248.1; 427/255.7; 427/397.7; 427/79; 438/240	Bronner; Gary Bela et al.
US 5876266 A	19990302	Polishing pad with controlled release of desired micro- encapsulated polishing agents	451/36	216/88; 252/79.1; 438/692	Miller; Matthe Kilpatrick et al
US 5795826 A	19980818	Method of chemically mechanically polishing an electronic component	438/692	216/89; 257/E21.304; 257/E21.583	Gambino; Jeffi Peter et al.
US 5795819	19980818	Integrated pad and fuse	438/618	257/E23.15;	Motsiff; Willia

A		structure for planar copper metallurgy		438/622; 438/623; 438/626; 438/627; 438/642; 438/687; 438/688	Thomas et al.
US 5792703 A	19980811	Self-aligned contact wiring process for SI devices	438/620	257/E21.507; 438/624; 438/637; 438/639	Bronner; Gary et al.
US 5781160 A	19980714	Independently fed AM/FM heated window antenna	343/713	343/704	Walton; Eric K
US 5766971 A	19980616	Oxide strip that improves planarity	438/296	148/DIG.50; 216/39; 216/58; 257/E21.252; 257/E21.546; 438/424; 438/437; 438/699	Ahlgren; David et al.
US 5760674 A	19980602	Fusible links with improved interconnect structure	337/297	257/529; 257/E23.15; 337/152; 337/293; 337/295	Gilmour; Richard A. et al.
US 5759867 A	19980602	Method of making a disposable corner etch stop-spacer for borderless contacts	438/639	257/E21.162; 257/E21.477; 257/E21.575; 438/702; 438/740; 438/970	Armacost; Michael D. et al.
US 5731624 A	19980324	Integrated pad and fuse structure for planar copper metallurgy	257/529	257/762; 257/763; 257/764; 257/766; 257/774; 257/E23.15	Motsiff; William Thomas et al.
US 5723898 A	19980303	Array protection devices and method	257/529	257/209; 257/665; 257/758	Gilmour; Richard Alfred et al.
US 5719070 A	19980217	Metallization composite having nickel intermediate/interface	438/614	257/E21.508; 257/E29.146; 438/654; 438/656	Cook; Herbert et al.
US 5622596	19970422	High density selective	438/702	216/39;	Armacost; Michael

A		SiO.sub.2 :Si.sub.3 N.sub.4 etching using a stoichiometrically altered nitride etch stop		257/E21.25; 438/970	D. et al.
US 5573633 A	19961112	Method of chemically mechanically polishing an electronic component	438/533	216/38; 216/88; 257/E21.304; 257/E21.58; 438/629; 438/633; 438/692	Gambino; Jeff P. et al.
US 5523253 A	19960604	Array protection devices and fabrication method	438/601		Gilmour; Rich A. et al.
US 5457345 A	19951010	Metallization composite having nickle intermediate/interface	257/766	257/761; 257/762; 257/763; 257/764; 257/765; 257/767; 257/768; 257/E21.508; 257/E23.021; 257/E29.146	Cook; Herbert et al.
US 5447599 A	19950905	Self-aligned process for capping copper lines	216/17	148/217; 216/51; 216/62; 216/78; 257/E21.582; 257/E21.584; 257/E21.591; 438/643; 438/648; 438/660	Li; Jian et al.
US 5420455 A	19950530	Array fuse damage protection devices and fabrication method	257/529	257/209; 257/665; 257/758; 365/225.7	Gilmour; Rich A. et al.
US 5383088 A	19950117	Storage capacitor with a conducting oxide electrode for metal-oxide dielectrics	361/305	257/306; 257/310; 257/E21.008; 257/E21.648; 361/311; 361/322; 427/126.3; 427/79	Chapple-Sokol Jonathan D. et
US 5355144	19941011	Transparent window	343/713	343/767;	Walton; Eric K

A		antenna		343/769	al.
US 5338702 A	19940816	Method for fabricating tungsten local interconnections in high density CMOS	438/620	257/E21.256; 257/E21.311; 257/E21.59; 438/648; 438/669; 438/720; 438/740; 438/970	Kobeda; Edward al.
US 5310602 A	19940510	Self-aligned process for capping copper lines	428/432	257/E21.584; 257/E21.591; 428/209; 428/75; 428/76	Li; Jian et al.
US 5298784 A	19940329	Electrically programmable antifuse using metal penetration of a junction	257/529	257/530; 257/751; 257/768; 257/771; 257/E23.147; 257/E23.149	Gambino; Jeffrey P. et al.
US 5286572 A	19940215	Planarizing ladder-type silsequioxane polymer insulation layer	428/447	257/40; 257/E21.26; 257/E21.261; 257/E23.119; 428/429; 428/448; 528/10; 528/38; 528/43	Clodgo; Donna et al.
US 5266504 A	19931130	Low temperature emitter process for high performance bipolar devices	438/364	117/8; 148/DIG.1; 148/DIG.124; 257/E21.131; 257/E21.133; 257/E21.371; 257/E21.379; 438/365	Blouse; Jeffrey et al.
US 5256597 A	19931026	Self-aligned conducting etch stop for interconnect patterning	438/625	257/E21.309; 257/E21.311; 257/E21.582; 438/642; 438/652; 438/658; 438/669; 438/740; 438/742;	Gambino; Jeffrey P.

				438/945; 438/970	
US 5251806 A	19931012	Method of forming dual height solder interconnections	228/180.22	228/254; 257/E21.511; 257/E23.021; 427/265; 427/97.3; 438/127; 438/652	Agarwala; Birendra N. et
US 5154514 A	19921013	On-chip temperature sensor utilizing a Schottky barrier diode structure	374/178	257/43; 257/467; 257/473	Gambino; Jeffi P. et al.
US 5134460 A	19920728	Aluminum bump, reworkable bump, and titanium nitride structure for tab bonding	257/737	257/733; 257/771; 257/915; 257/E21.516; 257/E23.021	Brady; Michael et al.
US 5130779 A	19920714	Solder mass having conductive encapsulating arrangement	257/772	257/737; 257/762; 257/763; 257/E21.511; 257/E23.021	Agarwala; Birendra N. et
US 4981530 A	19910101	Planarizing ladder-type silsesquioxane polymer insulation layer	438/780	148/33.3; 257/E21.26; 257/E21.261; 257/E23.119	Clodgo; Donna et al.
US 4840302 A	19890620	Chromium-titanium alloy	228/123.1	228/254; 228/262.51; 257/751; 257/764; 257/766; 257/774; 257/E21.508; 257/E23.02; 428/610; 428/620; 428/628	Gardner; David et al.
US 4723978 A	19880209	Method for a plasma-treated polysiloxane coating	216/55	216/62; 216/67; 216/80; 257/E21.26; 427/491; 438/781; 438/970; 65/31; 65/901	Clodgo; Donna et al.
US 4606998	19860819	Barrierless high-	430/312	257/E21.024;	Clodgo; Donna

A		temperature lift-off process		257/E21.025; 257/E21.255; 257/E21.587; 430/313; 430/314; 430/315; 430/316; 430/317; 430/323; 430/324; 430/326; 430/327; 430/328; 430/329; 430/330; 438/670; 438/951	et al.
US 4590258 A	19860520	Polyamic acid copolymer system for improved semiconductor manufacturing	528/189	257/E21.259; 257/E23.119; 528/188	Linde; Harold et al.
US 4527445 A	19850709	Automatic control system having manual control engageable at will	74/625	251/129.03; 74/89.22	Walton; Eric K
US 4438662 A	19840327	Automatic control system having manual control engageable at will	74/625	137/85; 310/80; 74/89.37	Walton; Eric K al.
US 3968243 A	19760706	Substituted guanidine compounds in the treating of arrhythmias	514/634		Maxwell; Robt Arthur et al.
US 3949089 A	19760406	Substituted guanidine compounds as antifibrillatory agents	514/634		Maxwell; Robt Arthur et al.